

## "System On A Chip" or "System In A Package" That Is The Question

The idea of incorporating a very high degree of integration into a single solid state electronics system is very tempting from such stand-points as operational speed, fabrication efficiency and very high density of functionality. However these positive attributes come at a very high cost. There are complex questions with regard to the integration of vastly different fabrication processes, yield in fabricating a single system including such elements as MEMS, imbedded passives, digital and analog devices, and testability of the final unified system. The challenge for the packaging community is to develop integration technologies which enable the assembly of systems with interconnect densities comparable to those on silicon devices but which permit the individual fabrication of disparate technologies and enhance testability of both these individual devices and the system as a whole. These issues are particularly true for the spacecraft electronics. The System On A Chip project, at JPL, is developing a roadmap for the creation of efficient Systems In A Package which will advance currently available commercial technologies and, in conjunction with university and industry collaborators identify and develop the required advanced technologies.